REMARKS

The application has been carefully reviewed in light of the Office Action dated October 21, 2003. Claims 48-65 are currently pending. Claims 48, 51, 53, 55, 60 and 62-65 have been amended. Claims 66 and 67 have been added. Support for the additional claims can be found in the original specification, for instance, at p. 19, lines 13-20. Accordingly, no new matter has been added. Reconsideration and allowance are respectfully requested in light of the foregoing amendments and the remarks that follow.

35 U.S.C. § 112, first paragraph

Claims 62-65 stand rejected under 35 U.S.C. § 112, first paragraph, as "containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." (Office Action, p. 3). The rejection is traversed.

Specifically, claim 62 has been amended to recite "connecting said at least one polysilicon gate to a write row address line of a memory integrated circuit, said thyristor being adapted to connect through said write row address line to a voltage source." This connection is illustrated in FIGS. 10 and 11 and is described in the original specification on p. 14, lines 3+. Accordingly, no new matter has been added.

Claim 63 has been amended to recite "isolation regions" in the substrate, deleting the unsupported "channel" language, as requested by the Examiner.

For at least these reasons, withdrawal of this rejection is respectfully requested.

35 U.S.C. § 112, second paragraph

Claims 48-62, 64, and 65 stand rejected under 35 U.S.C. § 112, second paragraph, as "being indefinite for failing to particularly point out and distinctly claim the

subject matter which applicant regards as the invention." (Office Action, at p. 4). The rejections are traversed and reconsideration is respectfully requested.

With regard to the phrase "incorporating said multi-region thyristor in a memory device," the Applicant respectfully maintains that this step encompasses a positive limitation to the method of forming a circuit, as explained in the Amendment dated July 2, 2003 and in the telephonic interview conducted July 14, 2003. One of ordinary skill in the art would understand this method limitation as claimed. This language, however, has been deleted from the rejected claims in order to expedite the prosecution of this case. Withdrawal of this rejection is respectfully requested.

Next, the Applicant maintains that the phrase recited in claim 62, "for producing latch-up in said multi-region planar thyristor . . . said thyristor being adapted to connect through said write row address line to a voltage source for producing latch-up" is not indefinite. This phrase describes the gate that is formed in performing this step of the claimed method. As the M.P.E.P. states "a functional limitation is often used in association with an element, ingredient, or step of a process to define a particular capability or purpose that is served by the recited element, ingredient or step." § 2173.05(g) (citing In re Venezia, 530 F.2d 956 (CCPA 1976), for holding that the language "members adapted to be positioned" is an acceptable limitation complying with 35 U.S.C. § 112, second paragraph). For at least these reasons, withdrawal of this rejection is respectfully requested.

35 U.S.C. § 103(a)

Claims 48-65 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Pat. No. 5,346,838 to Ueno ("Ueno") in view of U.S. Pat. No. 4,861,731 to Bhagat ("Bhagat"). The rejection is traversed and reconsideration is respectfully requested.

The present invention relates to forming memory devices for storing information in one of two states, using bipolar latch-up and gated diode breakdown. The subject

matter of claims 48-65 would not have been obvious over Ueno in view of Bhagat at the time of invention. Specifically, the Office Action does not establish a *prima facie* case of obviousness, which requires "some motivation, either in the references themselves themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the reference teachings. . [and] the prior art reference (or references when combined) must teach or suggest all the claim limitations." M.P.E.P. § 2143.

Even if, *arguendo,* there was some motivation to combine the teachings of Ueno with the teachings of Bhagat, the combination does not render the claimed invention obvious. Neither Ueno nor Bhagat, whether considered alone or in combination, recite all the limitations of claimed invention. Claim 48, for instance, recites a method of forming a memory circuit comprising "forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode."

The Office Action relies on Bhagat as teaching "forming at least one gate overlying a single junction" thereby making a gated diode, as recited by claims 48 and 55. (Office Action, at p. 5). The Examiner regards the meeting of regions 36 and 45 as the claimed "single junction." Bhagat, however, discloses that numeral 36 represents "strips of low resistivity material. . .[to] electrically connect ring 32 with buried layer 26," which do not effectively form a diode. (Col. 4, lines 43-47). Bhagat does teach creating a p-n junction, but this occurs between the channel 45 and the region 28. (Col. 5, lines 58-60). This junction is buried in the substrate surface and does not have a polysilicon gate overlying it, as recited by claim 48.

For at least these reasons, claim 48 is allowable and withdrawal of the rejection is respectfully requested. Claims 49-54 depend from claim 48 and are allowable for at least these reasons and for the unique combinations recited therein.

Like claim 48, claim 55 recites a method of forming a memory device comprising "forming at least one polysilicon gate overlying a single junction of said multi-region planar thyristor thereby making said single junction a gated diode." For at least the reasons described above regarding the allowance of claim 48, withdrawal of this rejection is respectfully requested. Claims 56-61, 64, and 65 depend from claim 55 and are allowable for at least these reasons and for the unique combinations recited therein.

Claim 62 recites "connecting said at least one polysilicon gate to a write row address line of a memory integrated circuit." (Emphasis added). Neither of the cited references teaches or even suggests a write row address line or a memory integrated circuit, therefore, the references do not teach this claim limitation. The Office Action relies on the symbol "G" of Ueno as teaching a write row address line. (Office Action, at p. 7). This "G," however, represents a gate terminal for applying a control voltage to an insulated gate, and "G" does not represent a write row address line, as recited by claim 62. Ueno does not teach, suggest, or even mention a write row address line. For at least these reasons, withdrawal of this rejection is respectfully requested.

Similarly, claim 63 recites "mutually coupling at least two gates of said plurality of gates to a write row address line of said memory integrated circuit." (Emphasis added). Accordingly, claim 63 is likewise allowable. Withdrawal of the rejection of claim 63 is respectfully requested.

Moreover, the subject matter of claims 48-65 would not have been obvious over Ueno in view of Bhagat at the time of invention because there existed no objective motivation or reason to combine the two reference teachings, as required to support a *prima facie* case of obviousness. M.P.E.P. § 2143.

The Office Actions states that it would have been obvious to modify the insulated gate control thyristor of Ueno with the "gate overlying a single junction of Bhagat. . . in order to turn the thyristor off." (Office Action, at p. 7). One of ordinary skill in the art would not be motivated in this way, however, because Ueno teaches a

different method of turning off the thyristor structure. In the passage cited by the Office Action, Ueno discloses "The MCT is turned off as follows by a negative control voltage applied to the gate." (Col. 2, lines 46-47). Thus, there exists no objective motivation to modify the cited references as suggested. Instead, the Office Action appears to be using the claimed invention as a roadmap to modify the references as to arrive at the claimed invention in a way that is not suggested by either reference.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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